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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## ACTIVITY BASED LEARNING

Course Code \& Course Title
Year/Sem/Branch
Name of Faculty
Designation
Unit Title
Topic
LO
Bloom's Taxonomy Level
: 19EC303 - Digital Principles and System Design
: II / III Sem / ECE
: Dr. Sheeba Joice.C
: Professor \& Deputy Head / ECE
: Combinational Circuits
: Binary Multiplier
: To understand the concept of binary multiplication.
: Understand

| S.No. | Title | Description |
| :---: | :--- | :--- |
| 1 | Concept | $\begin{array}{l}\text { A binary multiplier is a combinational logic circuit } \\ \text { used in digital systems to perform the multiplication of } \\ \text { two binary numbers. }\end{array}$ |
| 2 | Challenges Faced | $\begin{array}{l}\text { The circuit is quite complex and learners will find it } \\ \text { difficult to grasp the concept when it is taught using } \\ \text { chalk and talk method. As it will be difficult to relate } \\ \text { the relationship between different circuits. }\end{array}$ |
| 3 | Name of the Activity | Fill the missing terms |
| 4 | $\begin{array}{l}\text { Description of the } \\ \text { Activity }\end{array}$ | $\begin{array}{l}\text { A sheet with circuit of binary multiplier, where few } \\ \text { terms were missing were given to the learners and the } \\ \text { learners should try to complete it. This will enable the } \\ \text { learner to think and do. They will understand the } \\ \text { working of the circuit easily and in lesser time. As they } \\ \text { are doing it on their own, they will remember it. }\end{array}$ |
| 5 | $\begin{array}{l}\text { Feedback from } \\ \text { Learners } \\ \text { (Consolidated) }\end{array}$ | $\begin{array}{l}\text { The feedback collected from students in class room. } \\ \text { - It helps us to learn the concept easily. } \\ \text { - Easy to understand } \\ \text { - Interactive learning is very useful. }\end{array}$ |
| - Team work helps us to improve the confidence |  |  |$\}$| level. |
| :--- |
| - Learning become very effective. |




## Evidences/Proofs

This is the activity sheet.


## Binary Multiplication

A binary multiplier is a combinational logic circuit used in digital systems to perform the multiplication of two binary numbers. These are most commonly used in various applications especially in the field of digital signal processing to perform the various algorithms.

Commercial applications like computers, mobiles, high speed calculators and some general-purpose processors require binary multipliers.

Compared with addition and subtraction, multiplication is a complex process. In multiplication process, the number which is to be multiplied by the other number is called as multiplicand and the number multiplied is called as multiplier.

## Binary Multiplication

Similar to the multiplication of decimal numbers, binary multiplication follows the same process for producing a product result of the two binary numbers. The binary multiplication is much easier as it contains only 0 s and 1 s . The four fundamental rules for binary multiplication are

```
0 < 0 = 0
0 > 1 =
1 < 0 = 0
1\times1=1
```

The multiplication of two binary numbers can be performed by using two common methods, namely partial product addition and shifting, and using parallel multipliers.

Before discussing about the types, let us look at the unsigned binary numbers multiplication process. Consider a two 4 bit binary numbers as 1010 and 1011, and its multiplication of these two is given as


## 1101110

From the above multiplication, partial products are generated for each digit in the multiplier. Then all these partial products are added to produce the final product value. In the partial product multiplication, when the multiplier bit zero, the partial product is zero, and when the multiplier bit is 1 , the resulted partial product is the multiplicand.

As similar to the decimal numbers, each successive partial product is shifted one position left relative to the preceding partial product before summing all partial products.

Therefore, this multiplication uses $n$-shifts and adds to multiply n -bit binary number. The combinational circuit implemented to perform such multiplication is called as an array multiplier or combinational multiplier.

## Parallel Binary Multiplier Circuit

Let us consider two unsigned 2-bit binary numbers A and B to generalize the multiplication process. The multiplicand A is equal to A 1 A 0 and the multiplier B is equal to B 1 B 0 . The figure below shows the multiplication process of two 2-bit binary numbers.

## Al A0

$\times$
B1 B0


This process involves the multiplication of two digits and the addition of digits with or without carry. After the multiplication of each bit to the multiplicand, partial products are generated, and then these products are added to produce the total sum which represents the binary multiplication value.

This multiplication is implemented by combinational circuit such that the multiplication is performed with AND gates whereas the addition is carried out by using half adders as shown in figure.

## Al A0

B1 B0


The first partial product is obtained by the AND gate which is nothing but a least significant bit of the multiplication result. Since the second partial product is shifted to the left position, the first partial second term and second partial product first term is added by half adder and produce the sum output along with the carry out.

This carry out is added at the next half adder as an input as shown in figure. Likewise, it produces the multiplication result of two binary numbers by using the simple circuit configuration. The multiplication of the two 2 bit number results a 4-bit binary number.

Let us consider two unsigned 4 bit numbers multiplication in which the multiplicand, A is equal to A3A2 A1A0 and the multiplier B is equal to B3B2B1B0. The partial products are produced depending on each multiplier bit multiplied by the multiplicand.

Each partial product consists of four product terms and these are shifted to the left relative to the previous partial product as shown in figure. All these partial products are added to produce the 8 bit product.


The logic circuit for the $4 \times 4$ binary multiplication can be implemented by using three binary full adders along with AND gates.

In the above operation the first partial product is obtained by multiplying B0 with A 3 A 2 A 1 A 0 , the second partial product is formed by multiplying B1 with A3A2 A1A0, likewise for 3rd and 4th partial products. So these partial products can be implemented with AND gates as shown in figure.

These partial products are then added by using 4 bit parallel adder. The three most significant bits of first partial product with carry (considered as zero) are added with second partial term in the first full adder.

Then the result is added to the next partial product with carry out and it goes on till the final partial product, finally it produces 8 bit sum which indicates the multiplication value of the two binary numbers.


